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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,506	05/11/2001	Mark L. Janecek	END920000132US1	6858

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EXAMINER

ALCALA, JOSE H

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/853,506

Applicant(s)

MARK L. JANECEK, JOHN S. KRESGE, MARK V. P

Examiner

Jose H Alcalá

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 10 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 11-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 11-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 May 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4. 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to because Reference number 12 in Figures 1-3, is labeled “signal core” while in the Specification it is labeled as “signal core layer”. In addition, Reference number 142 in Figures 1-3, is labeled “power core” while in the Specification it is labeled as “power core layer”. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
2. The drawings are objected to because in all figures there is a layer at the outside of the “signal core”, which is never labeled or mentioned in the Specification. In addition, there is a layer in the center of the “power core”, which is also never labeled or mentioned in the Specification. Correction is required.
3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first and second spaced apart substrates, where the first substrate comprises a pair of spaced-apart outer signal cores, and the first second substrate comprising an inner power core sandwiched between said pair of outer signal cores of claim 13, or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

4. The disclosure is objected to because of the following informalities: It is unclear if there is a difference between the "signal core layer" and the "signal core". In addition it is unclear if there is a difference between the "power core layer" and the "power core". The terms used in the specification need to be consistent with the terms used in the claims, in order to be clear and enabling. Appropriate correction is required.

5. The drawings are objected to because it is not clear if what is labeled as signal core and power core, are substrates or just layers. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding Claim 13, it is not clear in the Specification how can the second substrate which is spaced apart from the first substrate and having a third substrate laminated between them, can comprise an inner

Art Unit: 2827

power core sandwiched between a pair of spaced-apart outer signal cores comprised in the first substrate.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 3,4,7,11-14, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 3,7 and 13, it is not clear how can the first substrate (a single substrate) comprise a pair of spaced - apart signal cores. For examination purposes, the recitation "first substrate" is interpreted as being just a label for the pair of spaced-apart outer signal cores.

Regarding Claim 11, it is not clear if the first and second spaced-apart substrates comprise **both** a **single** signal core, or if **each** substrate comprises a signal core. For examination purposes, it is interpreted as each comprising a signal core.

Regarding Claim 13, it is further unclear how can the second substrate, which is spaced apart from the first substrate by having a third substrate laminated between them, comprise an inner power core sandwiched between a pair of spaced-apart outer signal cores comprised in the first substrate.

#### ***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2827

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-7,11-14 rejected under 35 U.S.C. 102(b) as being anticipated by Duffy et al (US Patent No. 5,876,842).

Regarding Claim 1, Duffy teaches a multi-layered circuit structure, comprising: a first substrate (top core of Figure 4) having conductive via through holes (Reference number 22) disposed therein; and a second substrate (middle core of Figure 4) laminated to said first substrate and having conductive, adhesive-filled via through holes (Reference number 22) that align with, and make electrical contact with, the conductive via through holes of said first substrate upon lamination of said first and second substrates.

Regarding Claim 2, Duffy teaches that the first substrate (top core of Figure 4) comprises a signal core, and said second substrate (middle core of Figure 4) comprises a power core.

Regarding Claim 3, as best understood by the examiner: Duffy teaches that the first substrate (the combination of top and bottom cores of Figure 4) comprises a pair of spaced-apart outer signal cores (top and bottom cores), and said second substrate comprises an inner power core (middle core) sandwiched between said pair of spaced-apart outer signal cores.

Regarding Claim 4, as best understood by the examiner: Duffy teaches that said via through holes (Reference number 22, of middle core of Figure 4) of said inner power core comprise undercut contact surfaces (the surfaces at the ends of plated through

Art Unit: 2827

hole 22 of the first substrate) and said via through holes (Reference number 22, of top and bottom core of Figure 4) of said pair of spaced apart signal cores have metallic pads (Reference number 18) that make electrical contact with said undercut contact surfaces of said via through holes of said inner power core.

Regarding Claim 5, Duffy teaches a multi-layered circuit structure, comprising: a first substrate (top core of Figure 4) having conductive via through holes (Reference number 22) disposed therein; and a second substrate (middle core of Figure 4) laminated to said first substrate, and having via through holes (Reference number 22) comprising conductive adhesive coated pads (Reference number 18 of the middle core, which are coated with reference number 36, which can be a conductive adhesive composite, see column 8, lines 59-62) that align with, and make electrical contact with, the conductive via through holes of said first substrate upon lamination of said first and second substrates.

Regarding Claim 6, Duffy teaches that said first substrate (top core of Figure 4) comprises a signal core, and said second substrate (middle core of Figure 4) comprises a power core.

Regarding Claim 7, as best understood by the examiner: Duffy teaches that the first substrate (the combination of top and bottom cores of Figure 4) comprises a pair of spaced-apart outer signal cores (top and bottom cores), and said second substrate comprises an inner power core (middle core) sandwiched between said pair of spaced-apart outer signal cores.

Regarding Claim 11, Duffy teaches a multi-layered circuit structure, comprising: first (top core of Figure 4) and second (bottom core of Figure 4) spaced-apart substrates, each having conductive via through holes (Reference number 22) disposed therein; and a third substrate (middle core of Figure 4) laminated between said first and second spaced-apart substrates and having conductive, adhesive filled via through holes (Reference number 22) that align with, and make electrical contact with, the conductive via through holes of said first and second spaced-apart substrates, upon lamination of said first and second spaced-apart substrates to said third substrate.

Regarding Claim 12, Duffy teaches that said first (top core of Figure 4) and second (bottom core of Figure 4) spaced-apart substrates comprise a signal core, and said third substrate comprises a power core (middle core of Figure 4).

### ***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duffy et al (US Patent No. 5,876,842). As best as the examiner is able to ascertain the invention:

Regarding Claim 13, Duffy teaches all the limitations of the instant claimed invention as stated supra for claim 11, but fails to explicitly teach that said first substrate



Art Unit: 2827

comprises a pair of spaced-apart outer signal cores, and said second substrate comprises an inner power core sandwiched between said pair of outer signal cores. Duffy teaches a substrate comprising a pair of spaced-apart outer signal cores (top and bottom cores of Figure 4), and a second substrate comprising an inner power core (middle core of Figure 4) sandwiched between said pair of outer signal cores. In addition, it is suggested by the Duffy reference (see claims 1 and 8) that the invention can comprise more than two signal cores and more than one power cores. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have more substrates laminated one to the other, and each one comprising more signal and power cores, thus making the circuit structure more robust to be able to mechanically support a potentially large amount of integrated circuit chips in close proximity, improving integration. In addition it would have been further obvious, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. See *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Regarding Claim 14, Duffy teaches via through holes (Reference number 22, of middle core of Figure 4) of said inner power core comprise undercut contact surfaces (the surfaces at the ends of plated through hole 22 of the first substrate) and said via through holes (Reference number 22, of top and bottom core of Figure 4) of said pair of spaced apart signal cores have metallic pads (Reference number 18) that make electrical contact with said undercut contact surfaces of said via through holes of said inner power core.

***Conclusion***

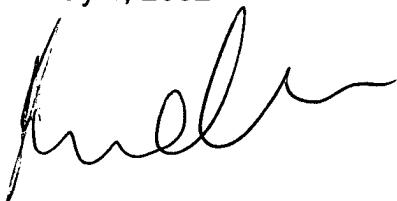
13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have some of the elements of the instant claimed invention: Chang et al (US Patent No. 5,774,340), Wiley (US Patent No. 5,142,775) and Davis et al (US Patent No. 5,280,414).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA  
May 4, 2002

A handwritten signature in black ink, appearing to read 'Kamand Cuneo', written over a horizontal line.

**KAMAND CUNEO  
PRIMARY EXAMINER**